

440LX DUAL PROCESSOR

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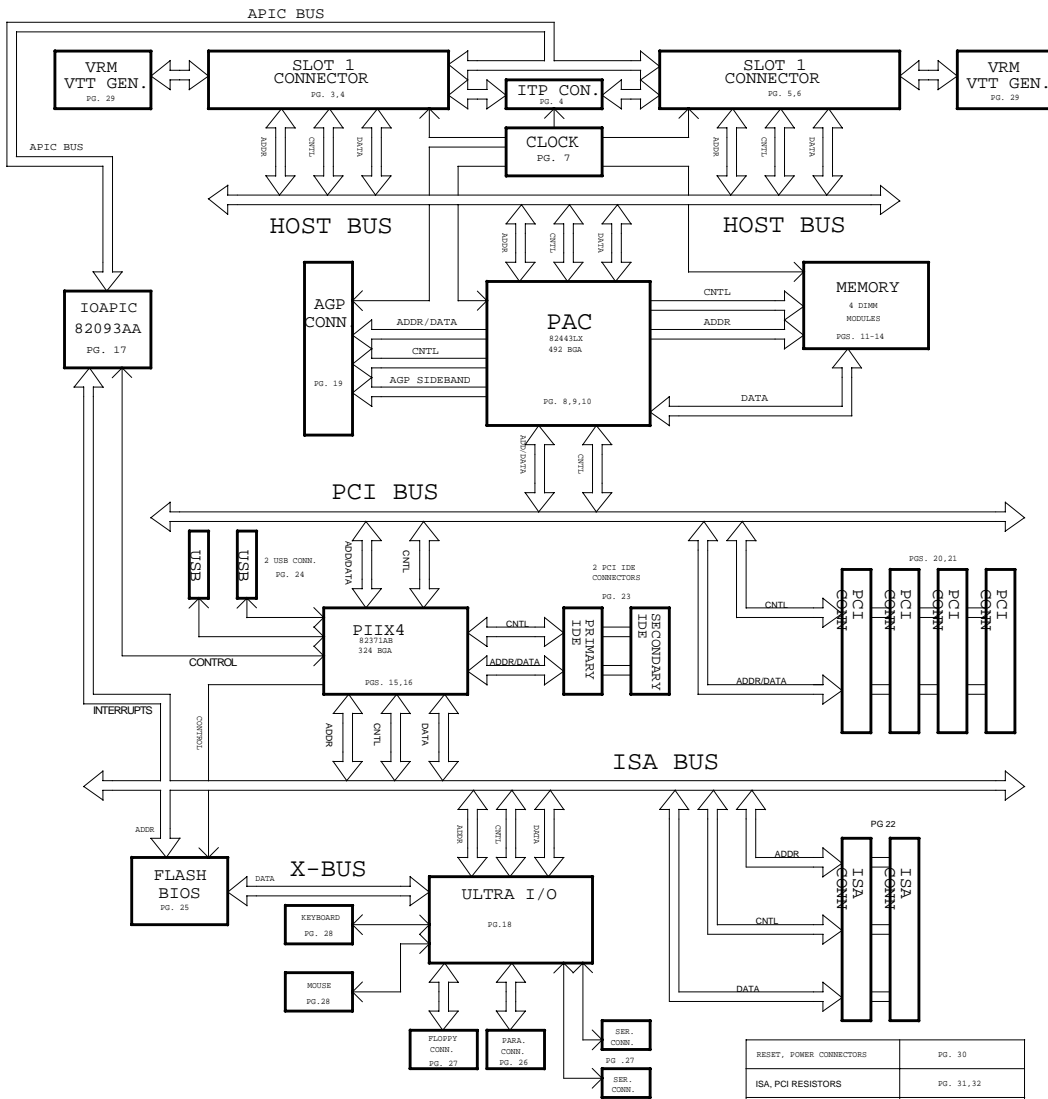
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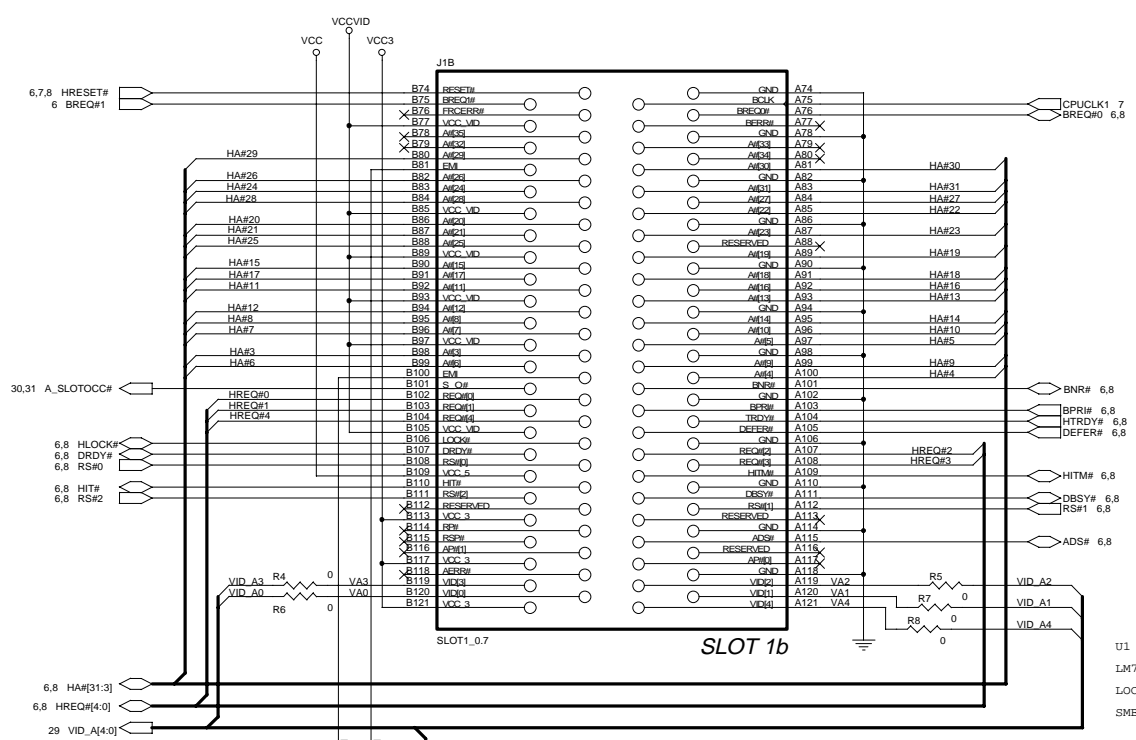
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Size A	Document Number Intel 440LX PCiset	Rev 0.5
Date:	Sheet 1 of 36	E

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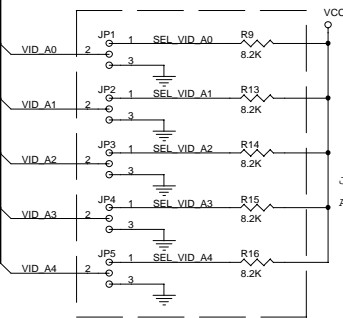


RESET, POWER CONNECTORS	PG. 30
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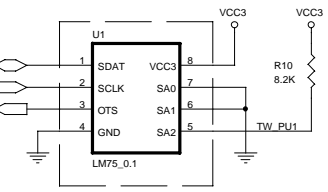
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File	440LX Block Diagram
Size	Document Number
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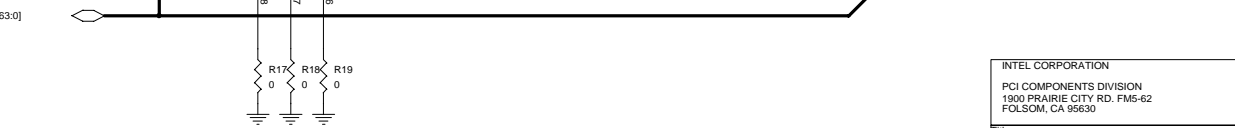
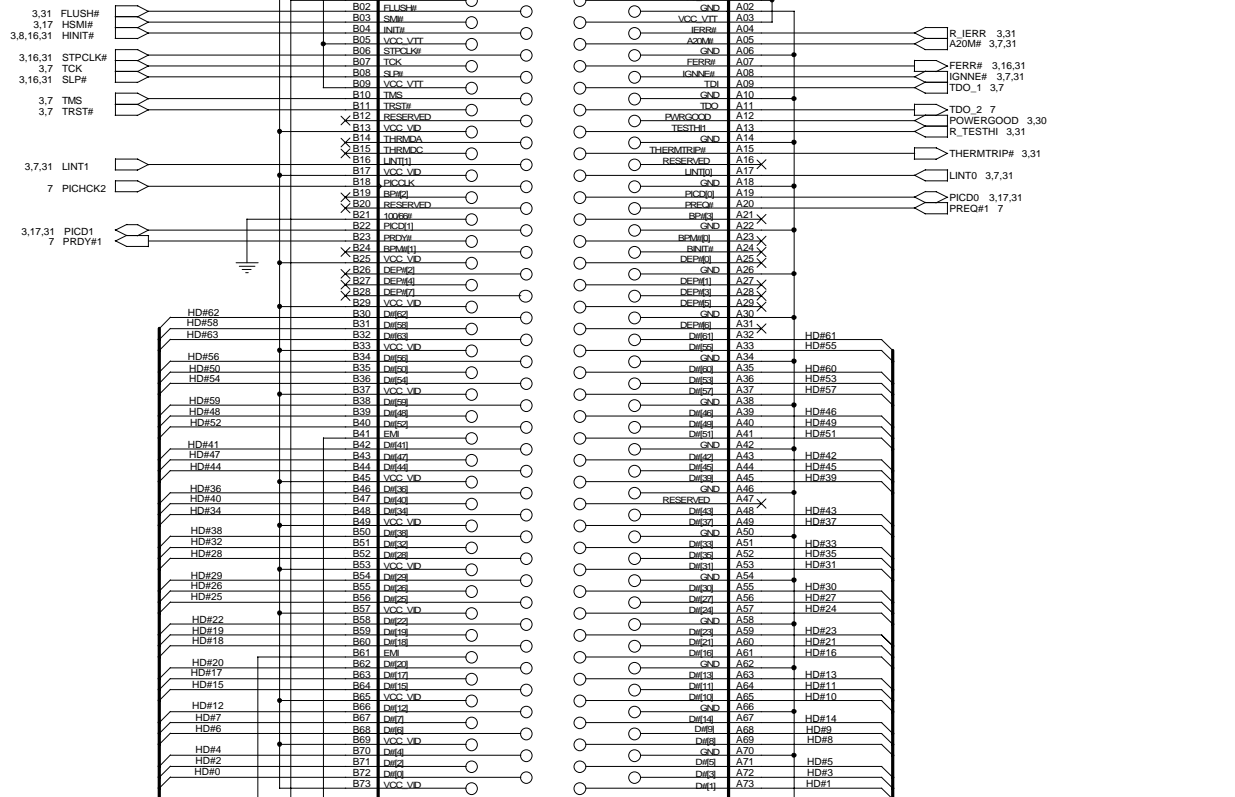
NOTE :
 U1 IS DEFAULT NO STUFF DEVICE.
 LM75 IS 3.3 VOLT THERMAL SENSOR.
 LOCATE NEAR THE CPU AND PAC.
 SMB SLAVE ADDRESS = 54H



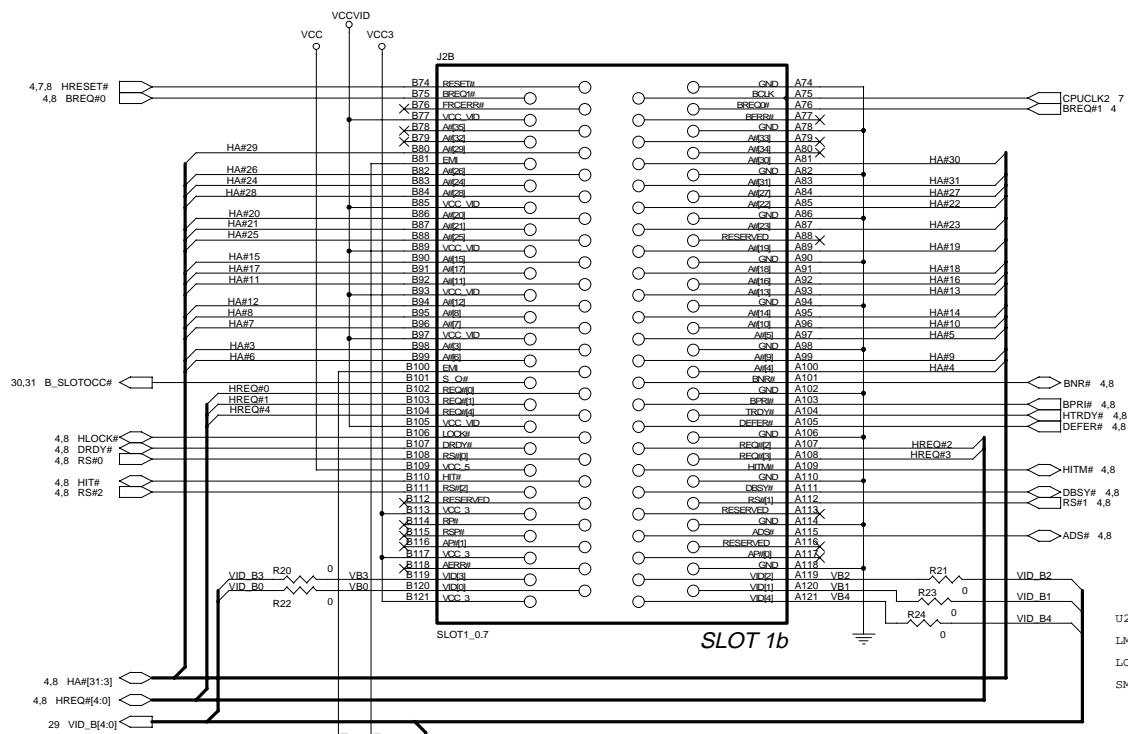
NOTE :
 JP1 - JP5 AND R9, R13-16
 ARE DEFAULT NO-STUFF



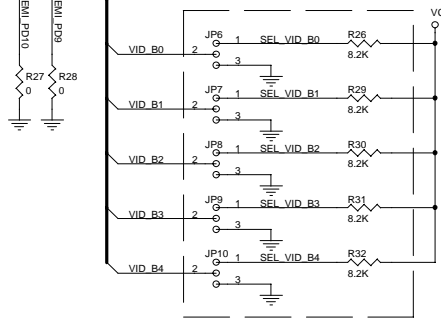
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Title FIRST SLOT 1 (PART II)		
Size	Document Number	Rev
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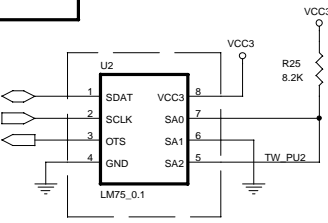
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PCI COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
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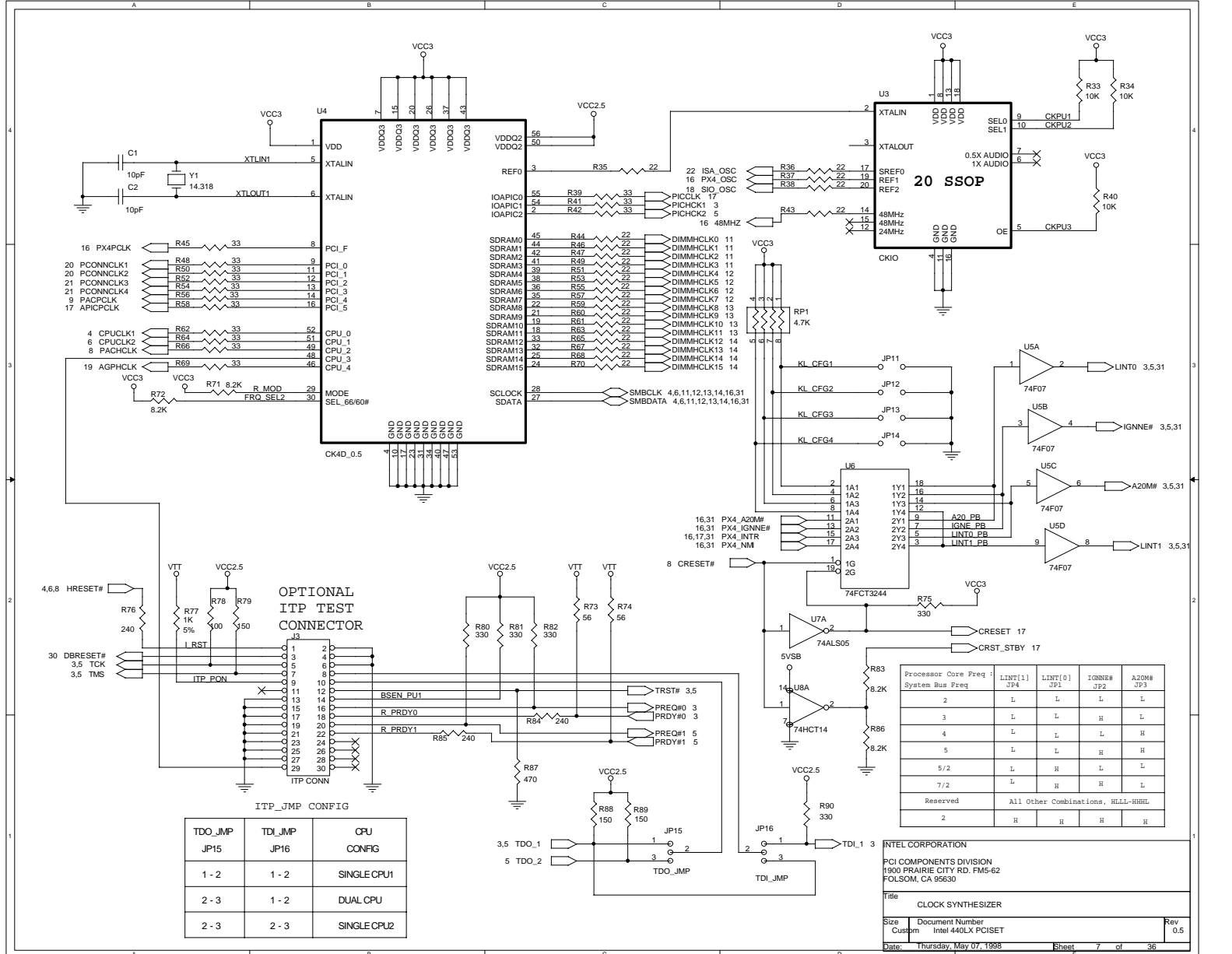
NOTE :
 U2 IS DEFAULT NO STUFF DEVICE.
 LM75 IS 3.3 VOLT THERMAL SENSOR.
 LOCATE NEAR THE CPU AND FAC.
 SMB SLAVE ADDRESS = 55H



NOTE :
 JP6 - JP10 AND R26, R29-32
 ARE DEFAULT NO-STUFF



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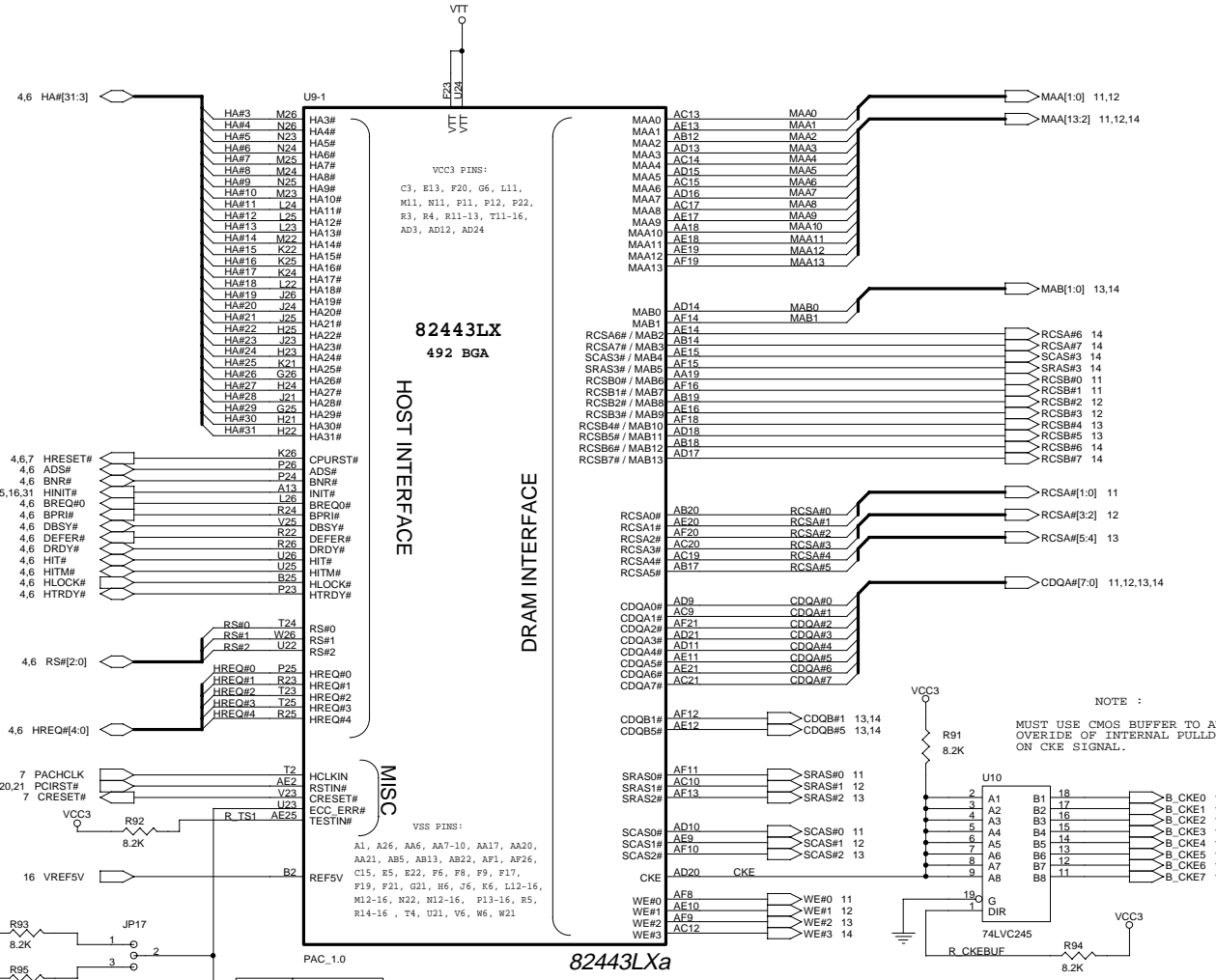
ITP_JMP CONFIG

TDO_JMP	TDI_JMP	CPU CONFIG
1 - 2	1 - 2	SINGLE CPU1
2 - 3	1 - 2	DUAL CPU
2 - 3	2 - 3	SINGLE CPU2

Processor Core Freq	System Bus Freq	LINT[1] JP4	LINT[0] JP1	IGNNE# JP2	A20M# JP3
2	L	L	L	L	L
3	L	L	L	H	L
4	L	L	L	L	H
5	L	L	L	H	H
5/2	L	H	L	L	L
7/2	L	H	H	L	L
Reserved	All Other Combinations, HLLL-HHLL				
2	H	H	H	H	H

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Title: CLOCK SYNTHESIZER
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VCC3 PINS:
C3, E13, F20, G6, L11,
M11, N11, P11, P12, P22,
R3, R4, R11-13, T11-16,
AD3, AD12, AD24

VSS PINS:
A1, A26, A6, AA7-10, AA17, AA20,
AA21, AB5, AB13, AB22, AP1, AP26,
C15, E5, E22, F6, F8, F9, F17,
F19, F21, G21, H6, J6, K6, L12-16,
M12-16, N22, N12-16, P13-16, R5,
R14-16, T4, U21, V6, W6, W21

NOTE:
MUST USE CMOS BUFFER TO AVOID
OVERIDE OF INTERNAL PULLDOWN
ON CKE SIGNAL.

NOTE:
CKE IS PULLED UP TO 3.3V FOR
CONFIGURATION 1.
SCHEMATICS WITH CONFIGURATION 2
SHOULD REMOVE PULLUP TO 3.3V.

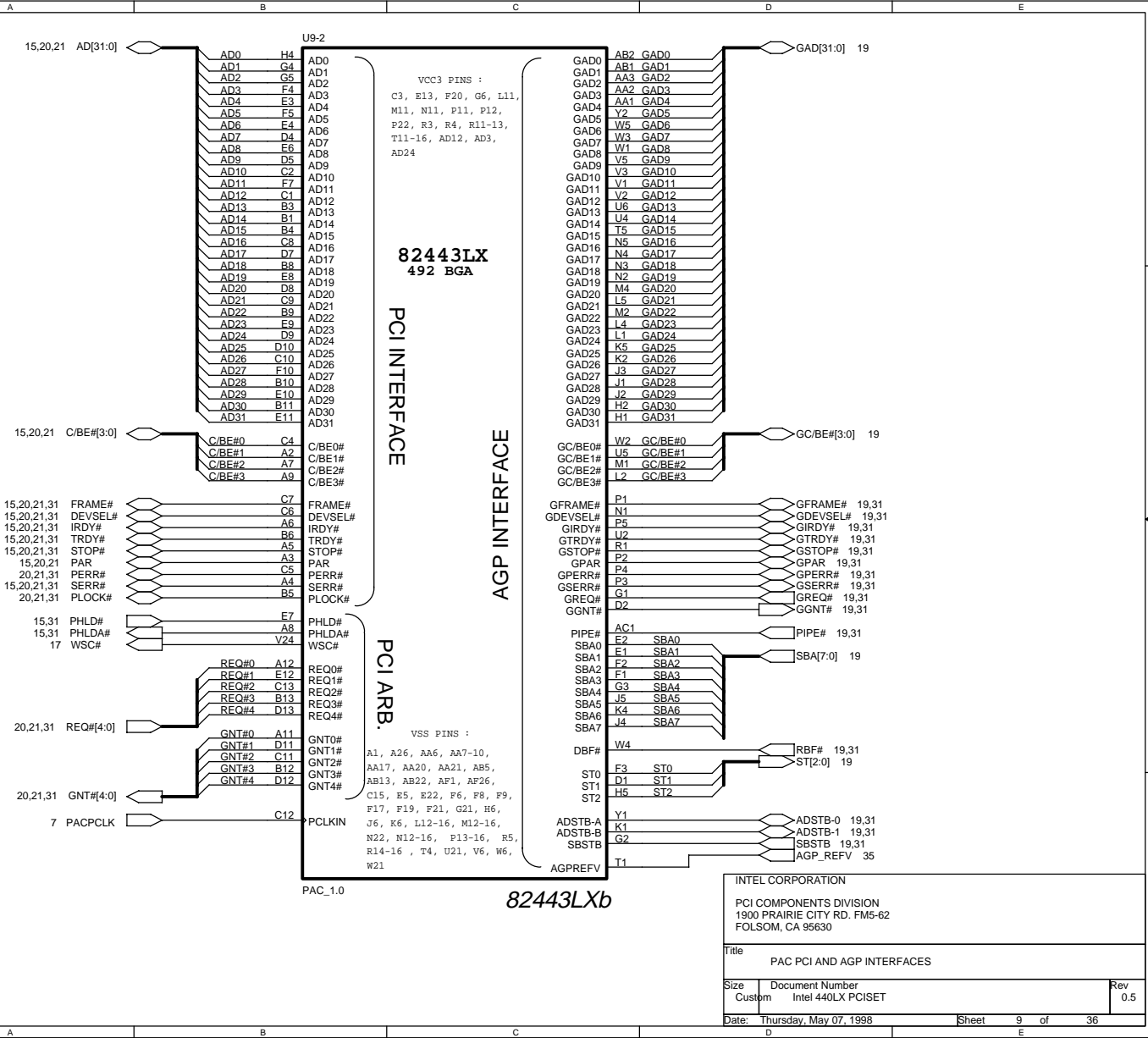
JP17	IOQ DEPTH
1-2	1
2-3	MAX

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Title: PAC HOST AND DRAM INTERFACES

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Title PAC PCI AND AGP INTERFACES		
Size Custom	Document Number Intel 440LX PCISSET	Rev 0.5
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11,12,13,14 MD[63:0]

U9-3

MD0	Y3
MD1	Y5
MD2	A25
MD3	AB4
MD4	AB6
MD5	AD1
MD6	AC3
MD7	AE1
MD8	AE3
MD9	AF3
MD10	AF4
MD11	AE5
MD12	AD6
MD13	AF6
MD14	AC7
MD15	AB8
MD16	AF23
MD17	AC22
MD18	AC23
MD19	AF25
MD20	AD25
MD21	AC24
MD22	AC26
MD23	AB23
MD24	AA22
MD25	AA24
MD26	AA25
MD27	Y22
MD28	Y24
MD29	Y25
MD30	W24
MD31	W25
MD32	AB3
MD33	AA4
MD34	AC2
MD35	Y6
MD36	AC4
MD37	AD2
MD38	AB7
MD39	AF2
MD40	AD4
MD41	AE4
MD42	AD5
MD43	AF5
MD44	AE6
MD45	AD7
MD46	AE7
MD47	AF7
MD48	AE23
MD49	AF24
MD50	AD23
MD51	AE26
MD52	AD26
MD53	AC25
MD54	AB24
MD55	AB25
MD56	AB26
MD57	Y21
MD58	AA26
MD59	W22
MD60	Y26
MD61	W23
MD62	Y22
MD63	V21
MECC0	AD8
MECC1	AE8
MECC2	AE22
MECC3	AE21
MECC4	AC8
MECC5	AB9
MECC6	AE22
MECC7	AD22

VCC3 PINS :
 C3, E13, F20, G6,
 L11, M11, N11, P11,
 P12, P22, R3, R4,
 R11-13, T11-16, AD12,
 AD3, AD24

82443LX
 492 BGA

MEMORY DATA BUS

HOST DATA BUS

VSS PINS :
 A1, A26, AA6, AA7-10,
 AA17, AA20, AA21,
 AB5, AB13, AB22, AF1,
 AF26, C15, E5, E22,
 F6, F8, F9, F17, F19,
 F21, G21, H6, J6, K6,
 L12-16, M12-16, N22,
 N12-16, P13-16, R5,
 R14-16, T4, U21, V6,
 W6, W21

HD0#	G22	HD#0
HD1#	G23	HD#1
HD2#	F25	HD#2
HD3#	G24	HD#3
HD4#	F24	HD#4
HD5#	F26	HD#5
HD6#	E26	HD#6
HD7#	F24	HD#7
HD8#	F22	HD#8
HD9#	E26	HD#9
HD10#	D25	HD#10
HD11#	G25	HD#11
HD12#	D26	HD#12
HD13#	B26	HD#13
HD14#	E23	HD#14
HD15#	D24	HD#15
HD16#	B24	HD#16
HD17#	A25	HD#17
HD18#	A23	HD#18
HD19#	A22	HD#19
HD20#	A24	HD#20
HD21#	B23	HD#21
HD22#	B22	HD#22
HD23#	D23	HD#23
HD24#	D22	HD#24
HD25#	C22	HD#25
HD26#	B21	HD#26
HD27#	A21	HD#27
HD28#	D20	HD#28
HD29#	E21	HD#29
HD30#	D21	HD#30
HD31#	C21	HD#31
HD32#	E20	HD#32
HD33#	B20	HD#33
HD34#	A19	HD#34
HD35#	A20	HD#35
HD36#	B19	HD#36
HD37#	D19	HD#37
HD38#	C20	HD#38
HD39#	F18	HD#39
HD40#	E18	HD#40
HD41#	C18	HD#41
HD42#	D17	HD#42
HD43#	E19	HD#43
HD44#	C19	HD#44
HD45#	B18	HD#45
HD46#	B17	HD#46
HD47#	E17	HD#47
HD48#	C17	HD#48
HD49#	A17	HD#49
HD50#	B15	HD#50
HD51#	D16	HD#51
HD52#	D18	HD#52
HD53#	C16	HD#53
HD54#	E16	HD#54
HD55#	D15	HD#55
HD56#	A14	HD#56
HD57#	B16	HD#57
HD58#	C14	HD#58
HD59#	A16	HD#59
HD60#	A15	HD#60
HD61#	D14	HD#61
HD62#	E15	HD#62
HD63#	B14	HD#63

HD#[63:0] 3,5

11,13,14 MECC[7:0]

GTL_REF
GTL_REF

C24
T22

PAC_GTLREF1 35
PAC_GTLREF2 35

PAC_1.0

82443LXc

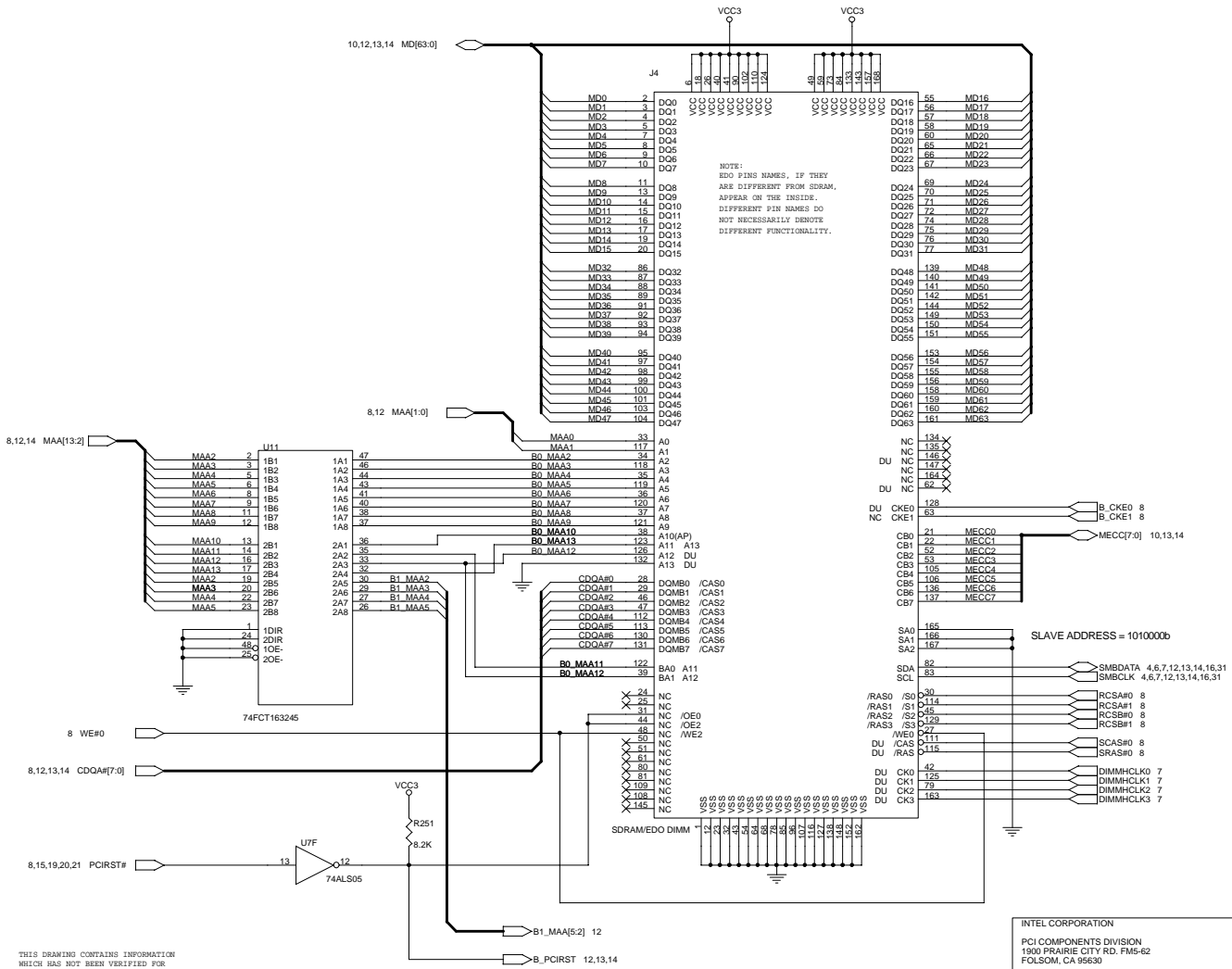
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Title: PAC DATA BUSES

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DIMM CONNECTOR 0

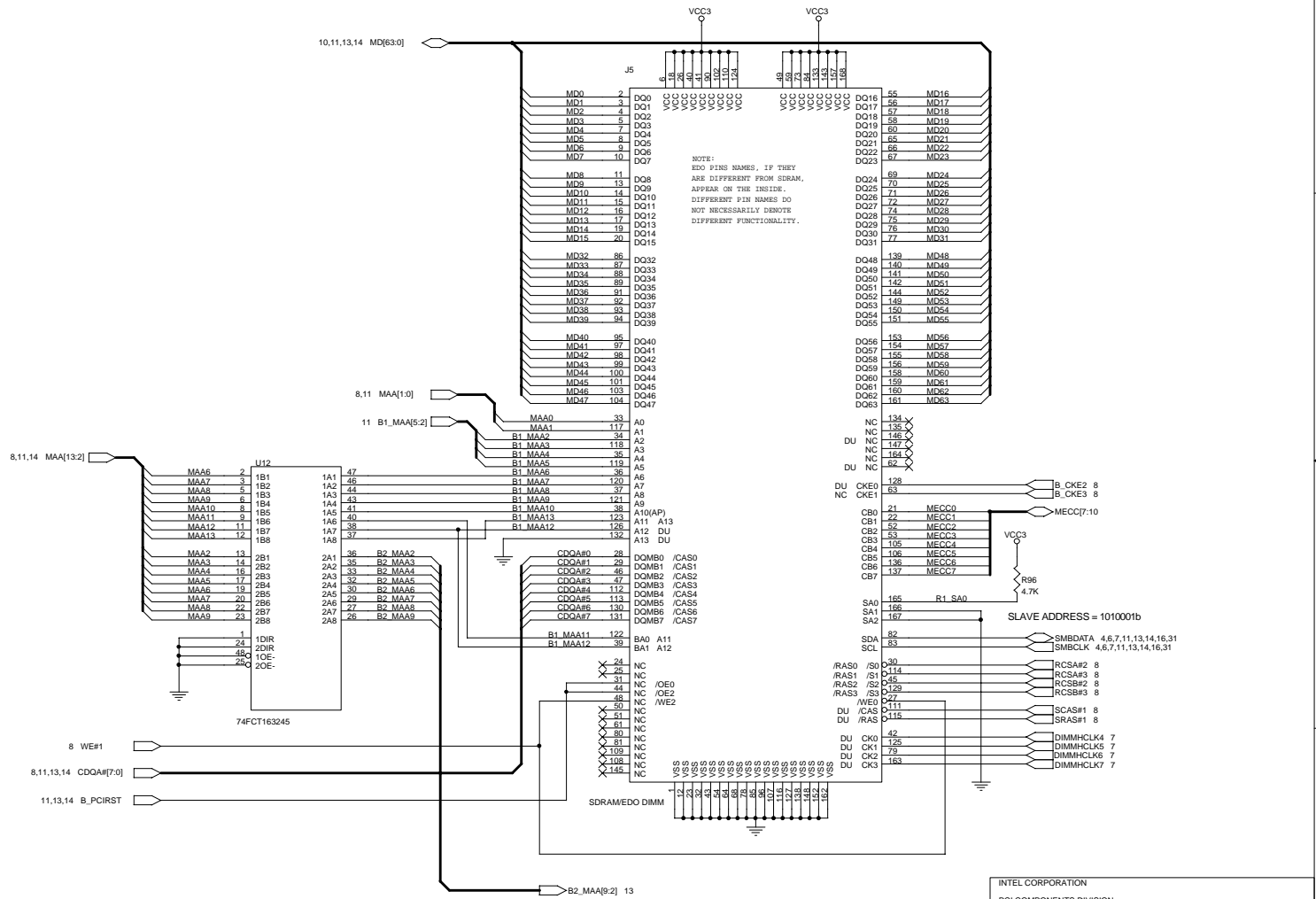


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Title		
FIRST DIMM SOCKET		
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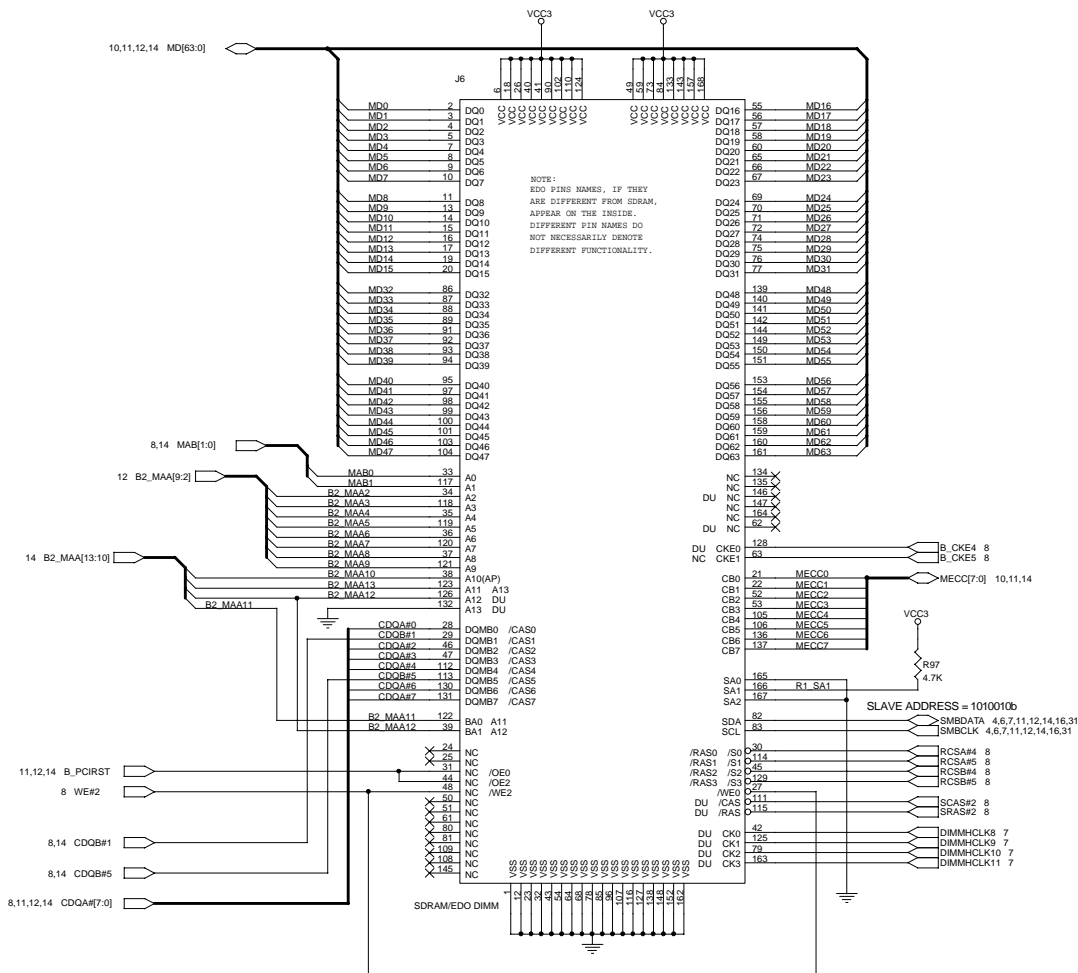
DIMM CONNECTOR 1



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DIMM CONNECTOR 2



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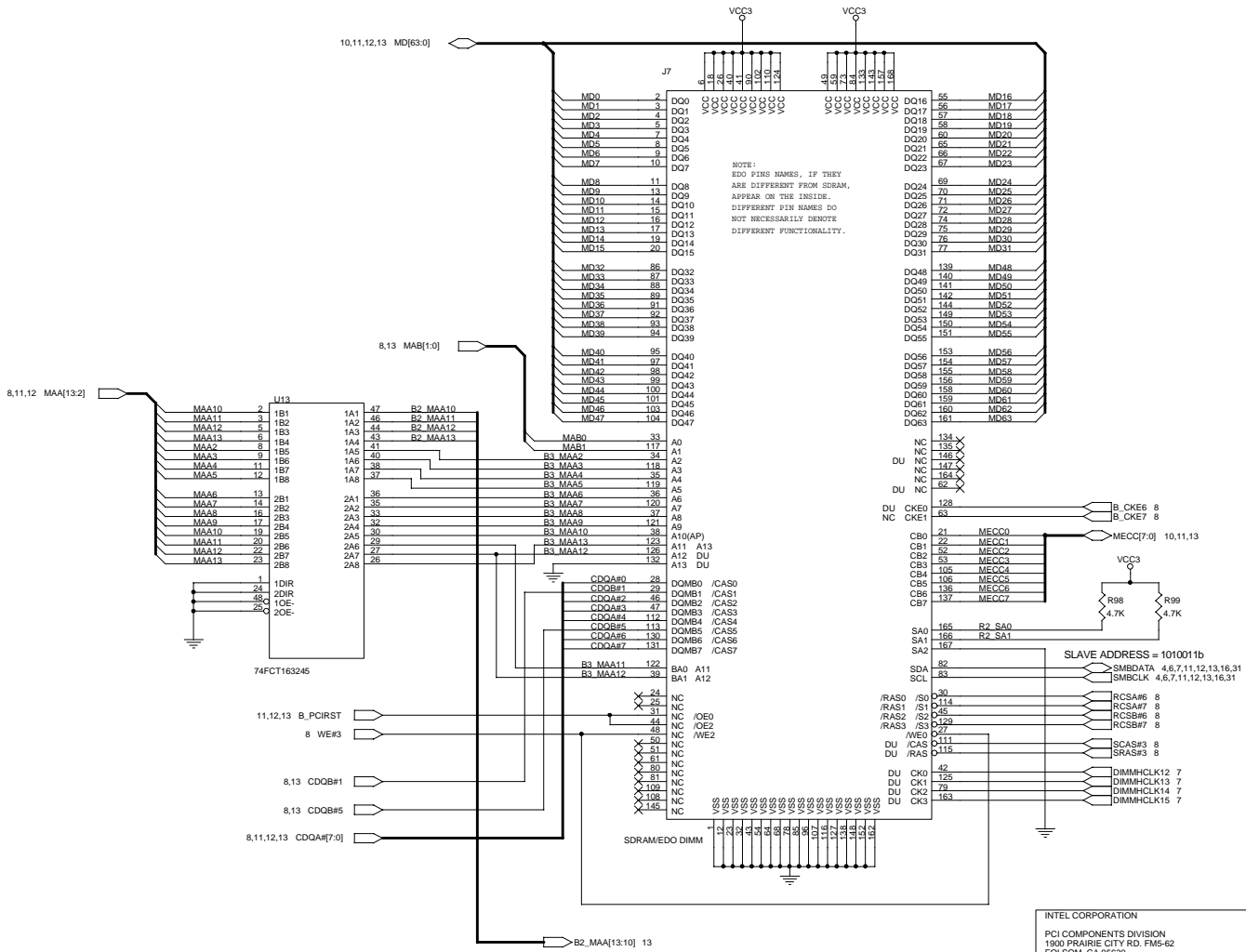
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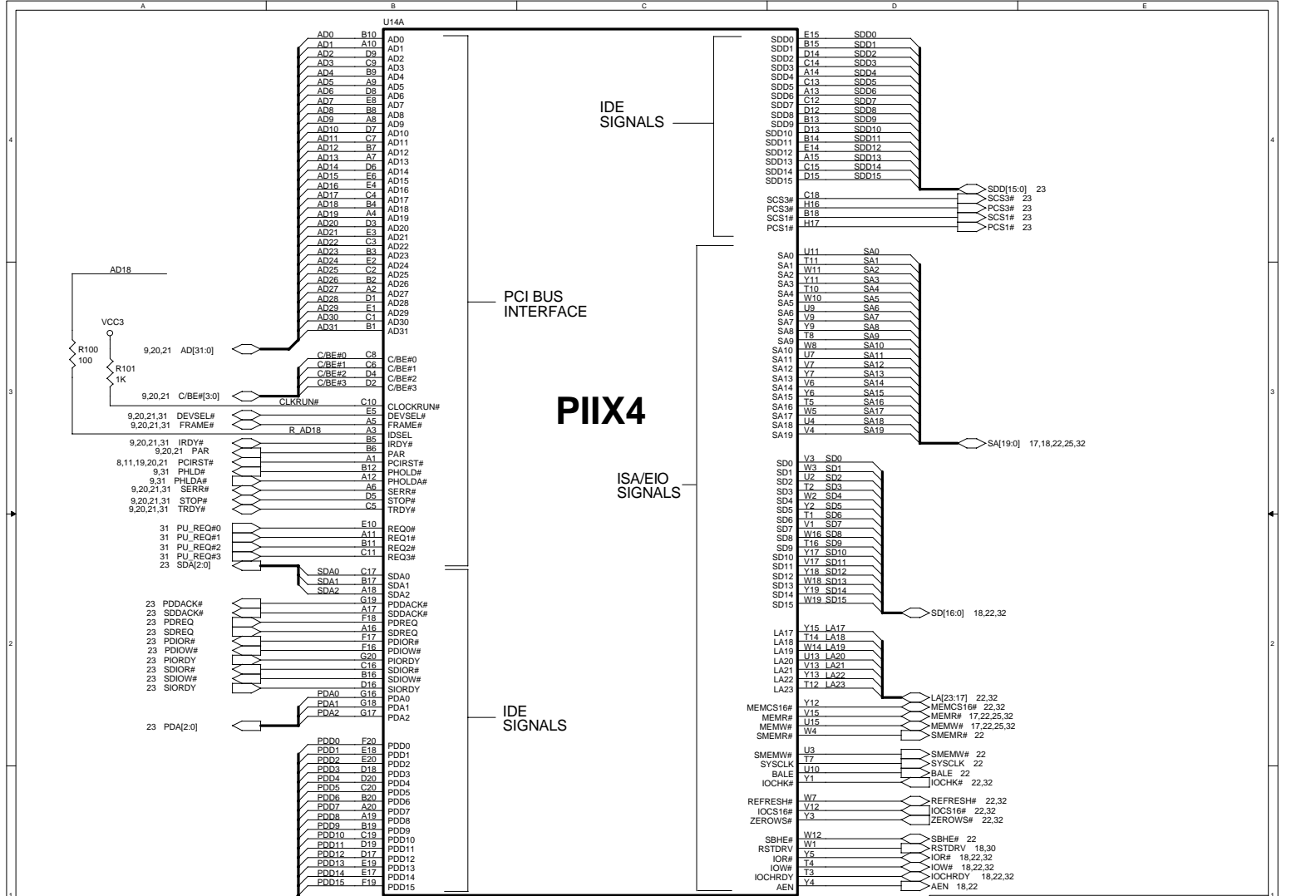
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Size	Document Number	Rev
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DIMM CONNECTOR 3

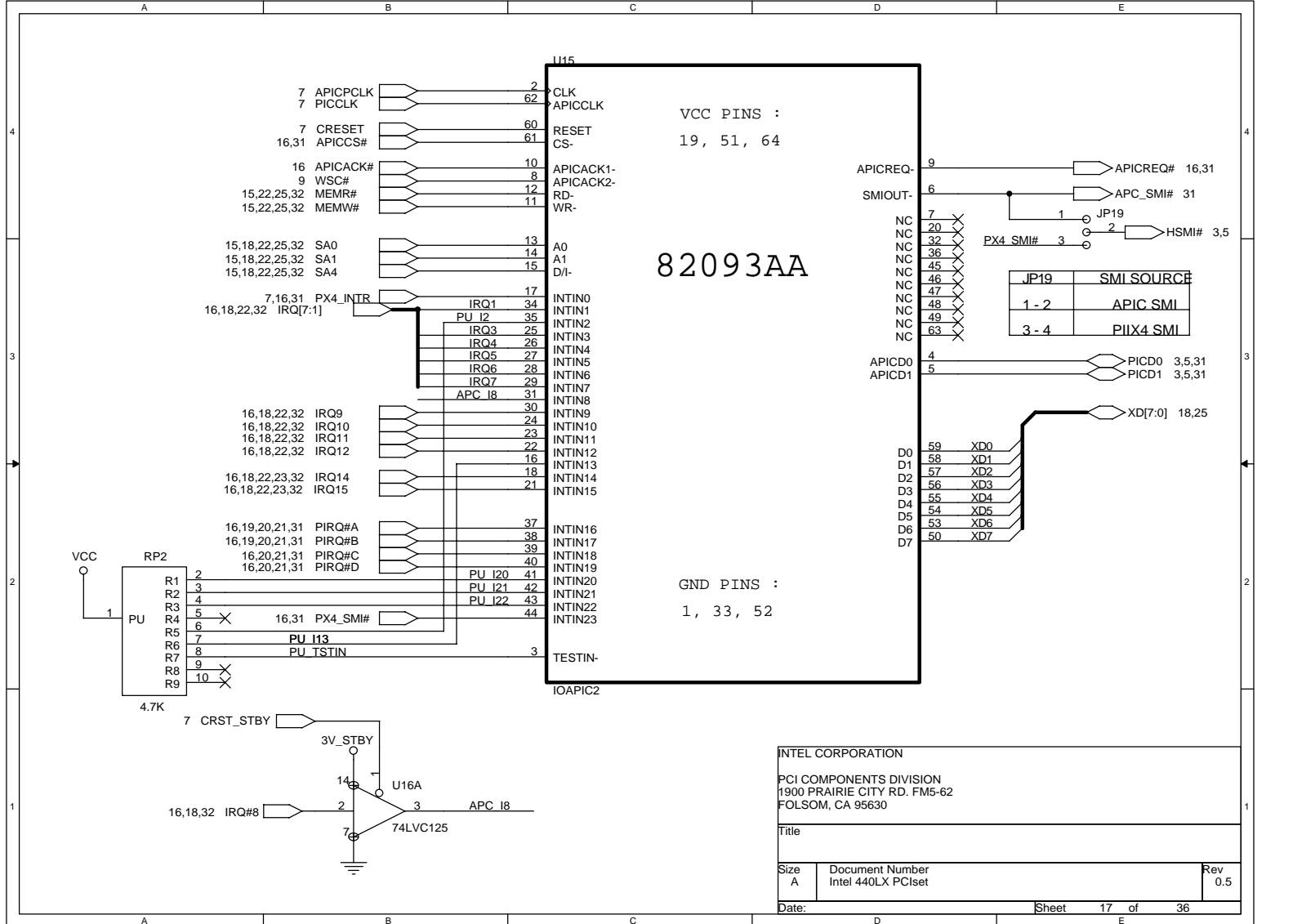




PIIX4

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file	PIIX4 (PART I)		Rev
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Custom	Intel 440LX PCISSET		
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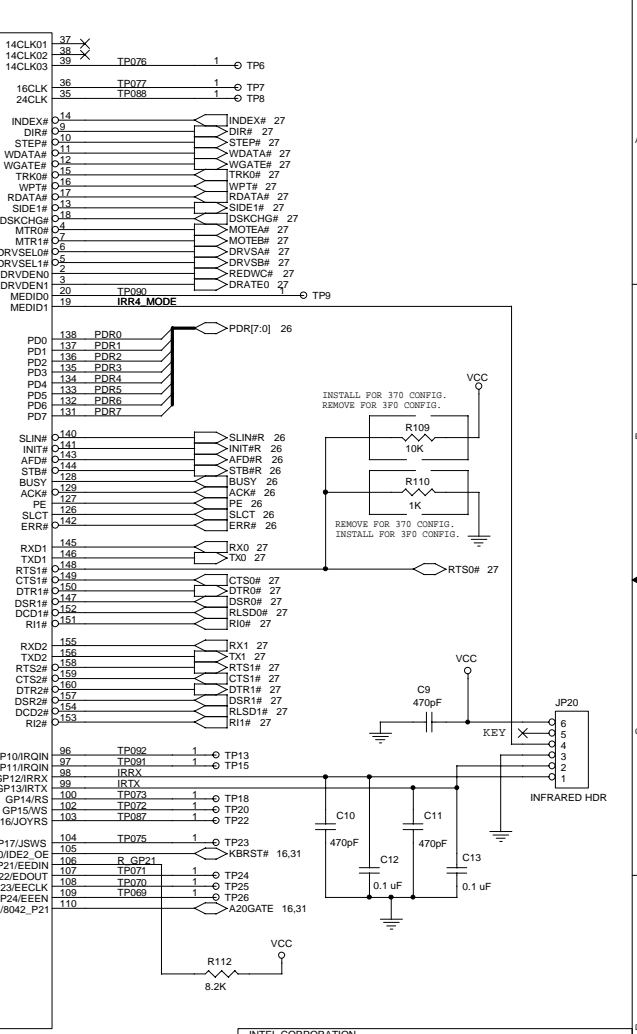
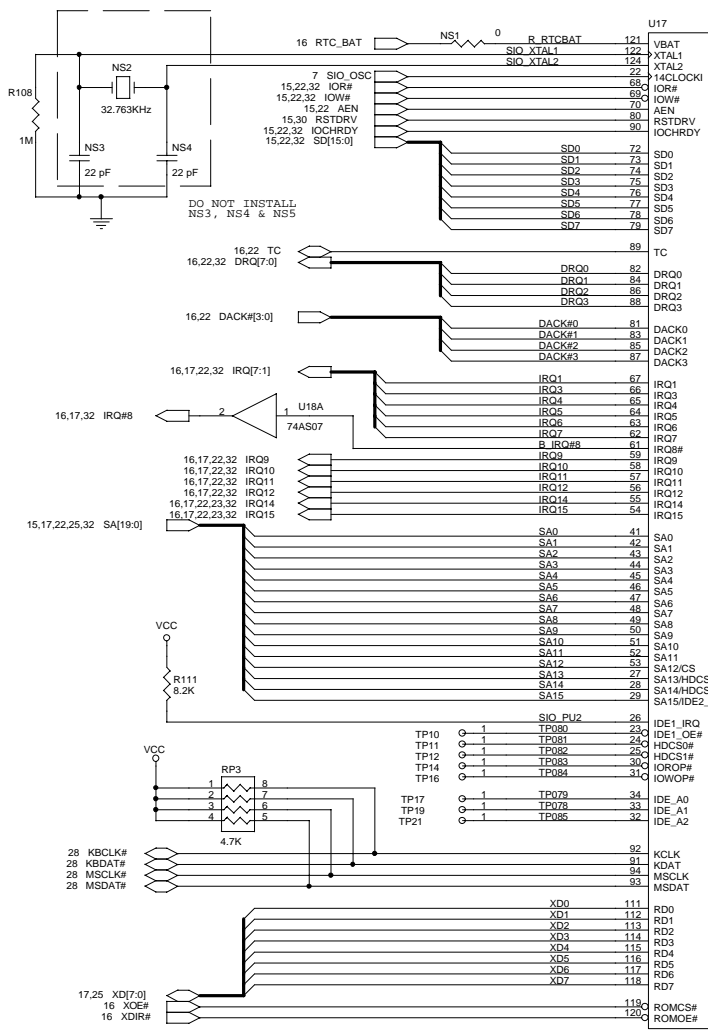


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Title

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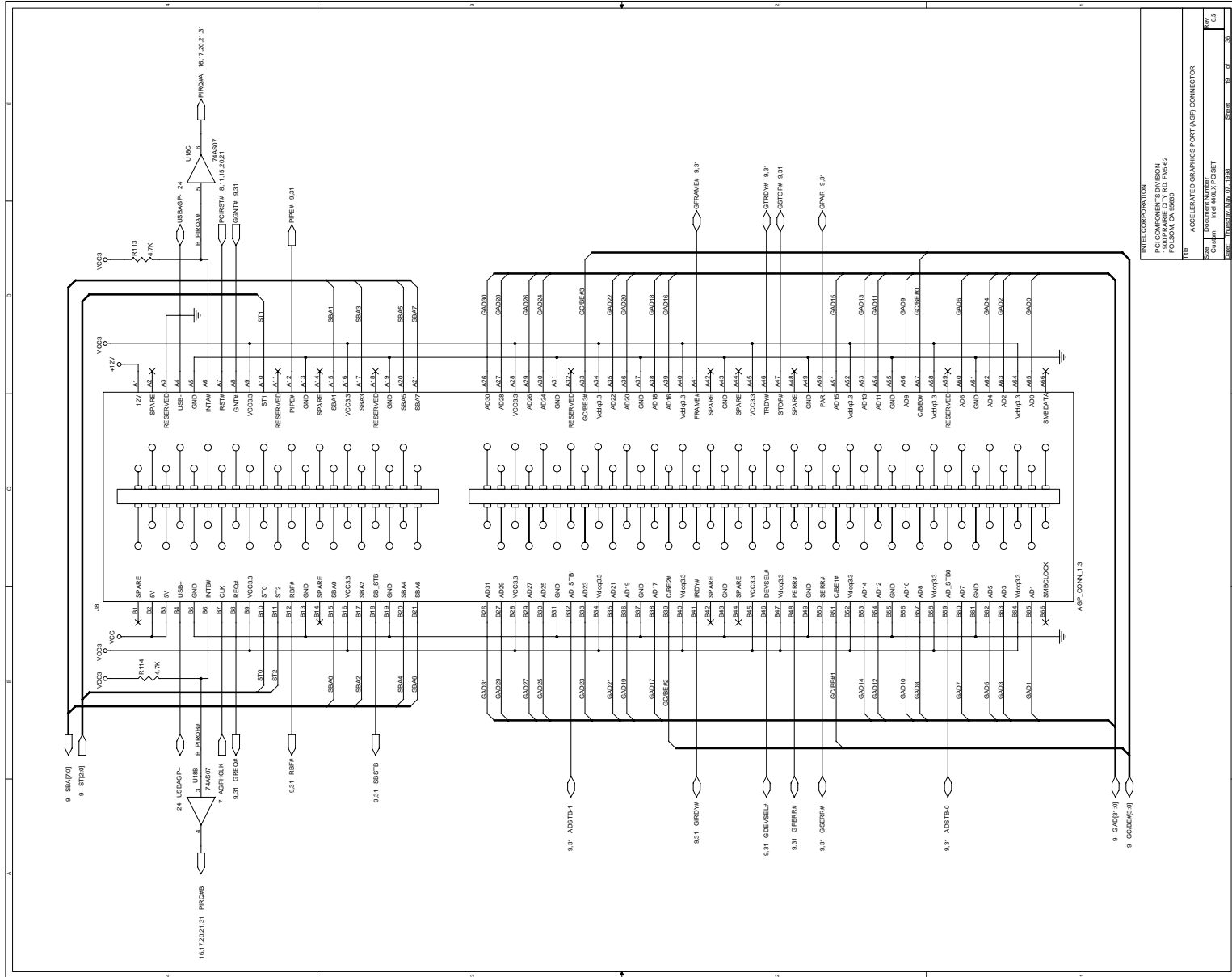


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ULTRA I/O

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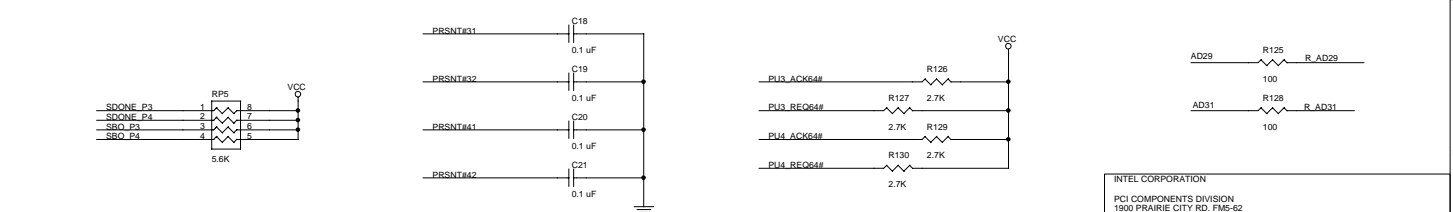
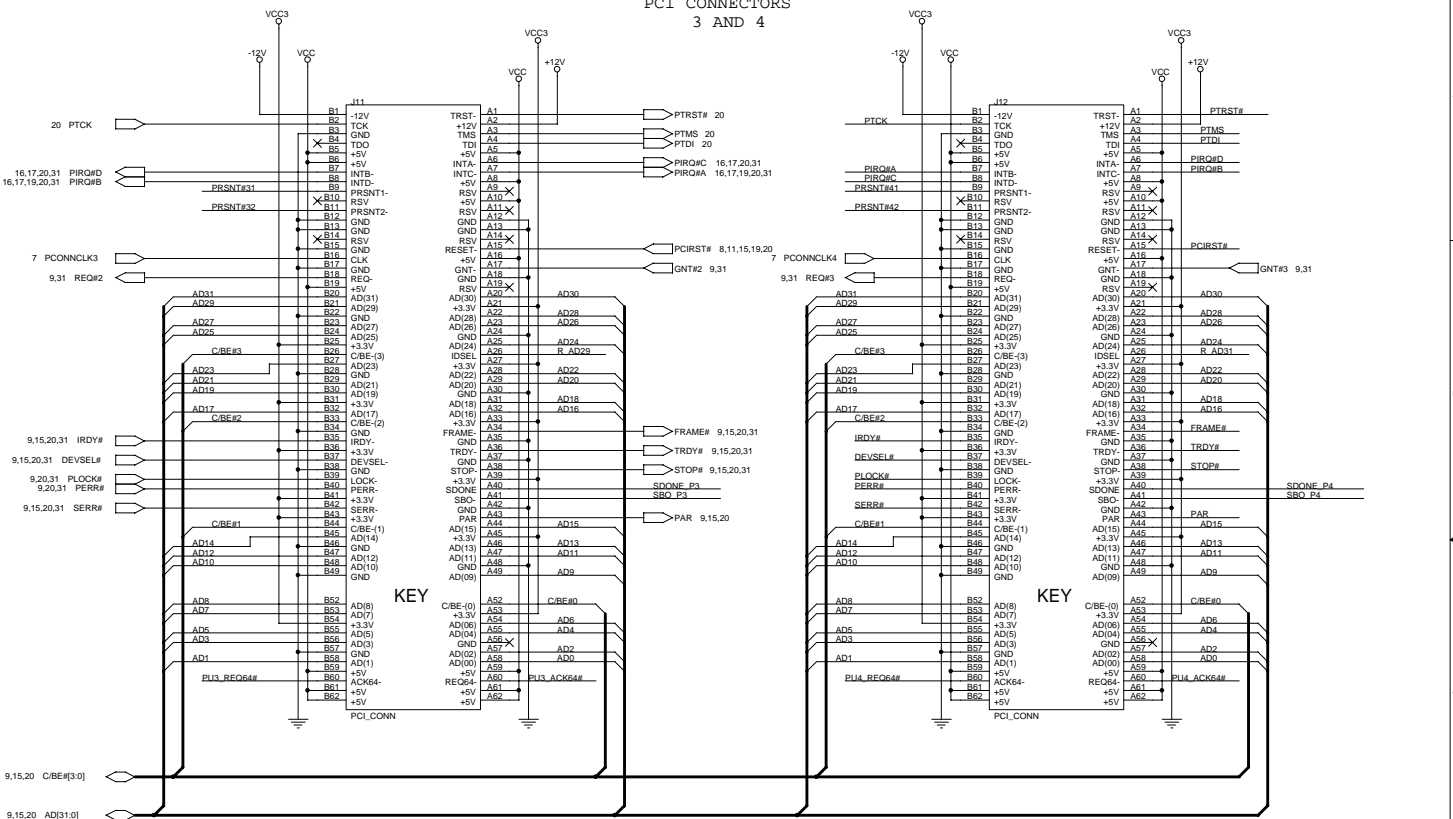
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Title: I/O CONTROLLER (ULTRA I/O)		
Size	Document Number	Rev
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 1900 PRIME CITY RD. #402
 FOLSOM, CA 95650
 TEL: 916.448.4000 FAX: 916.448.4001
 WWW: WWW.INTECCORP.COM

TITLE: ACCELERATED GRAPHICS PORT (AGP) CONNECTOR
 SIZE: 10.000 X 10.000 X 0.000
 DATE: 10/11/99
 DRAWN: J. W. WILSON
 CHECKED: J. W. WILSON
 APPROVED: J. W. WILSON
 SHEET: 13 OF 30

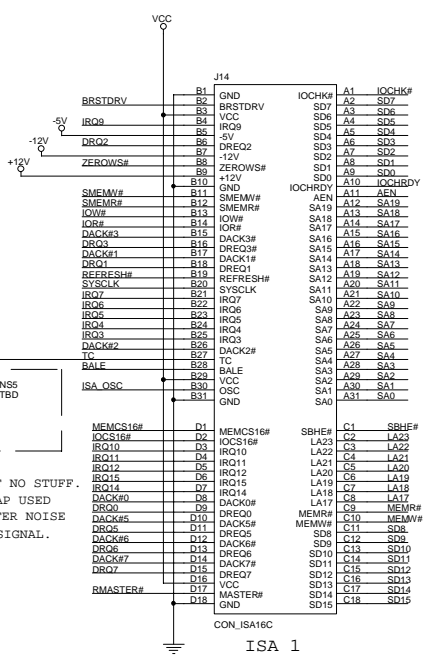
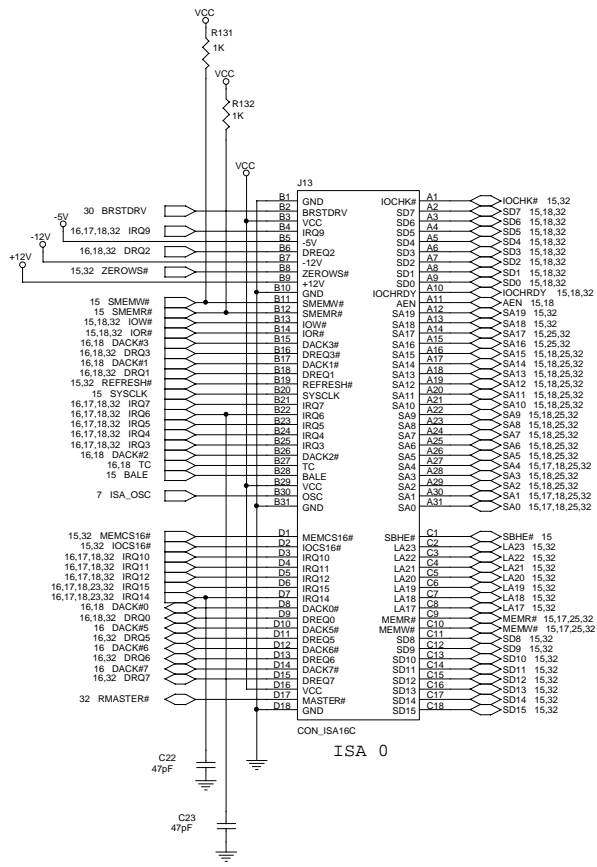
DO NOT REPRODUCE
PCI CONNECTORS
3 AND 4



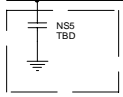
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ISA SLOTS



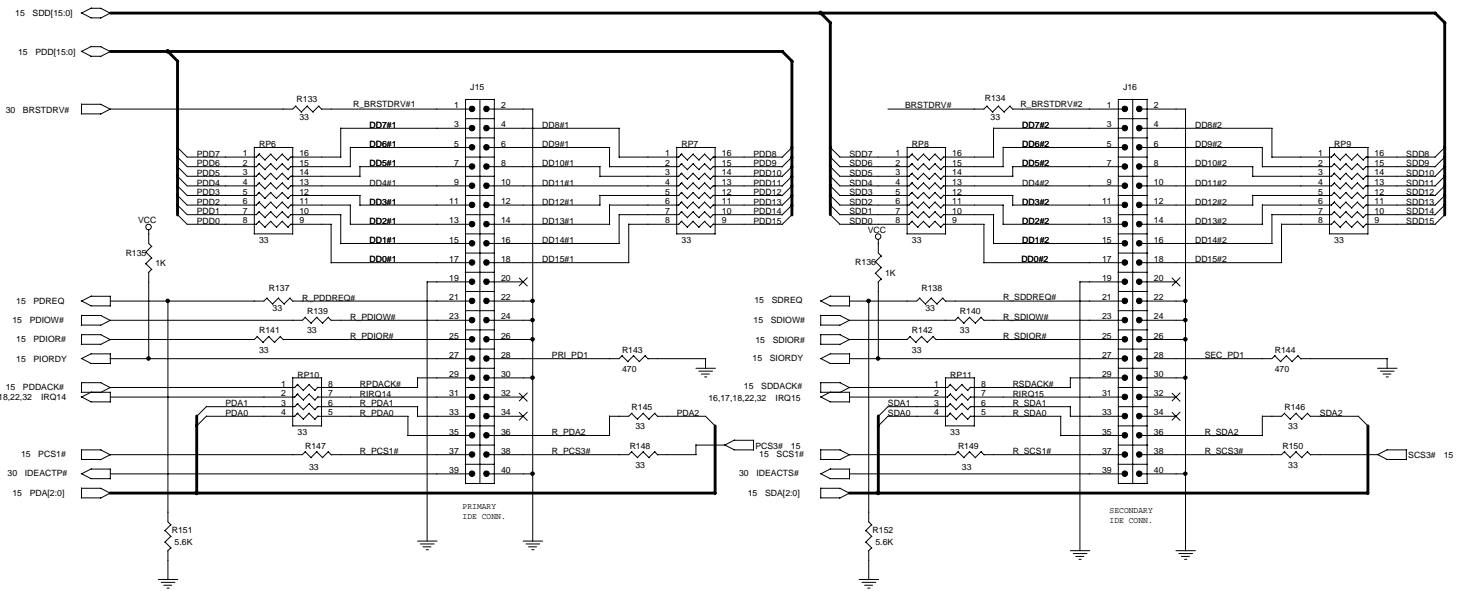
NOTE :
 DEFAULT NO STUFF.
 THIS CAP USED
 TO FILTER NOISE
 ON TC SIGNAL.



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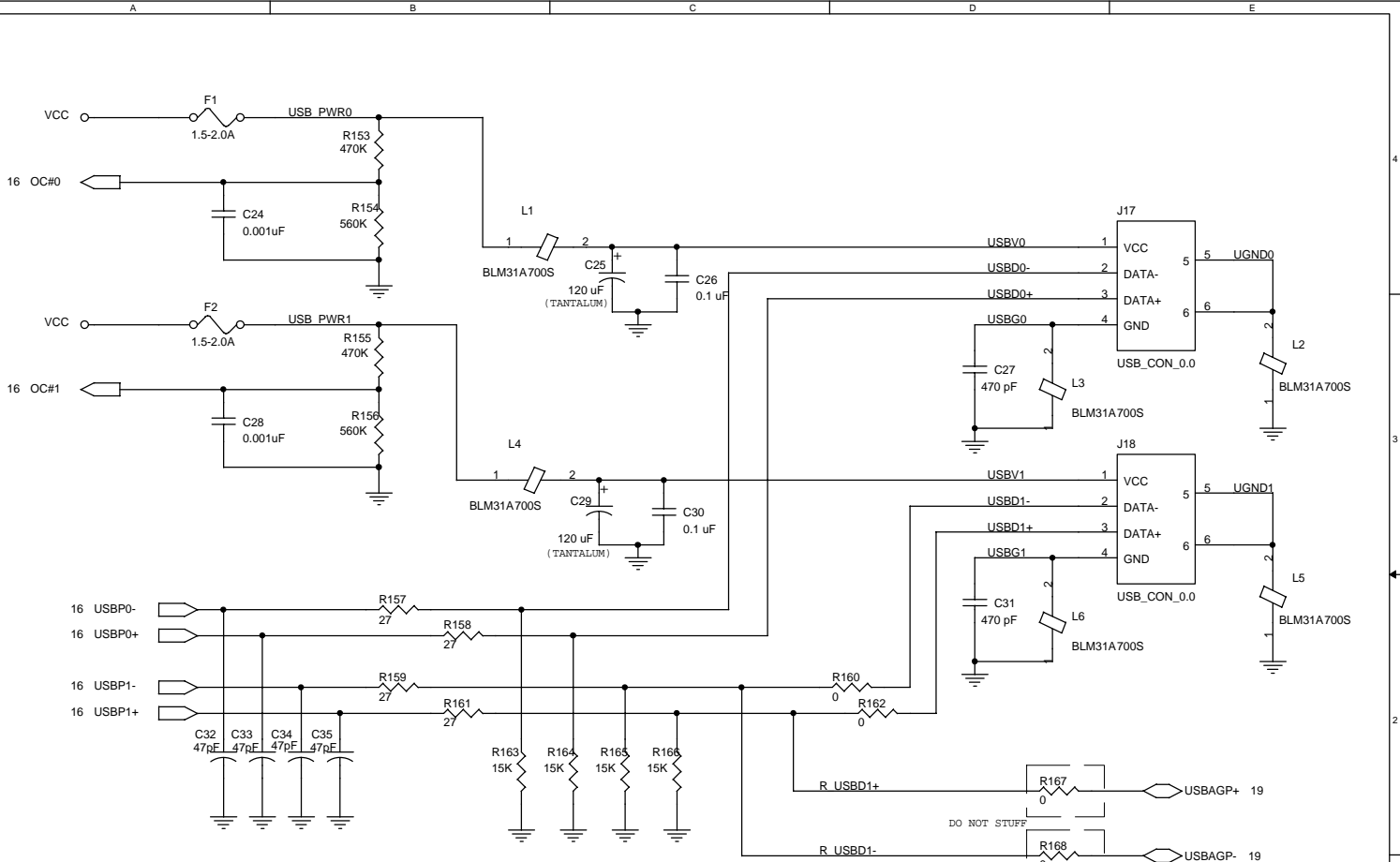
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Size	Document Number	Rev	
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IDE CONNECTORS



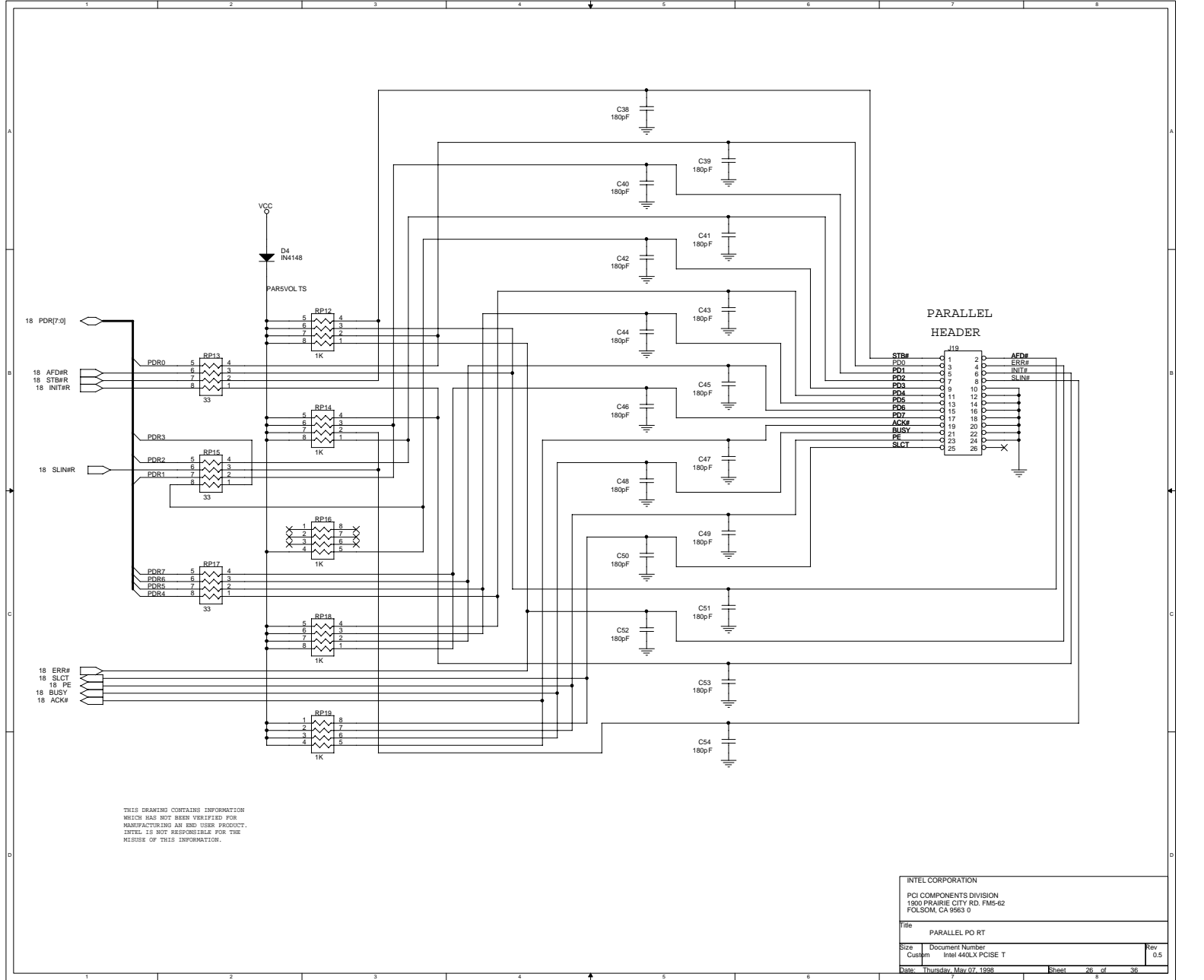
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File	PCI IDE CONNECTORS
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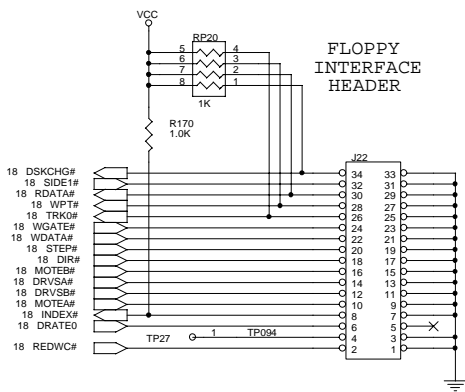
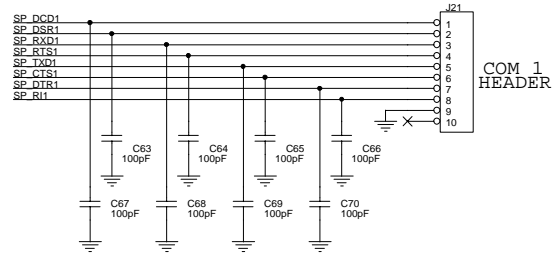
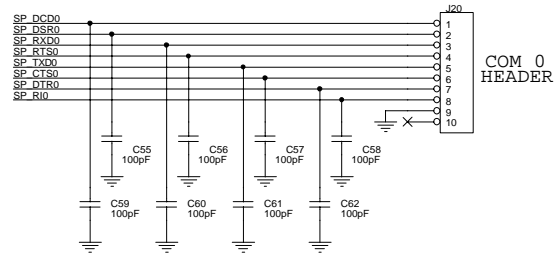
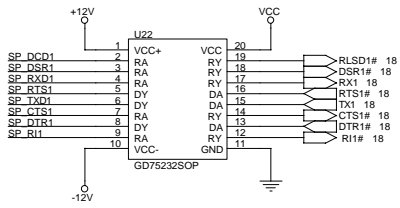
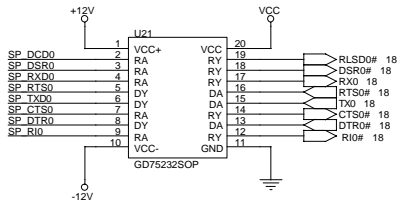
NOTE:
USE PIIx4
APPLICATION NOTE
FOR LAYOUT
GUIDELINES

INTEL CORPORATION		
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Title USB HEADER		
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Title	PARALLEL PORT	
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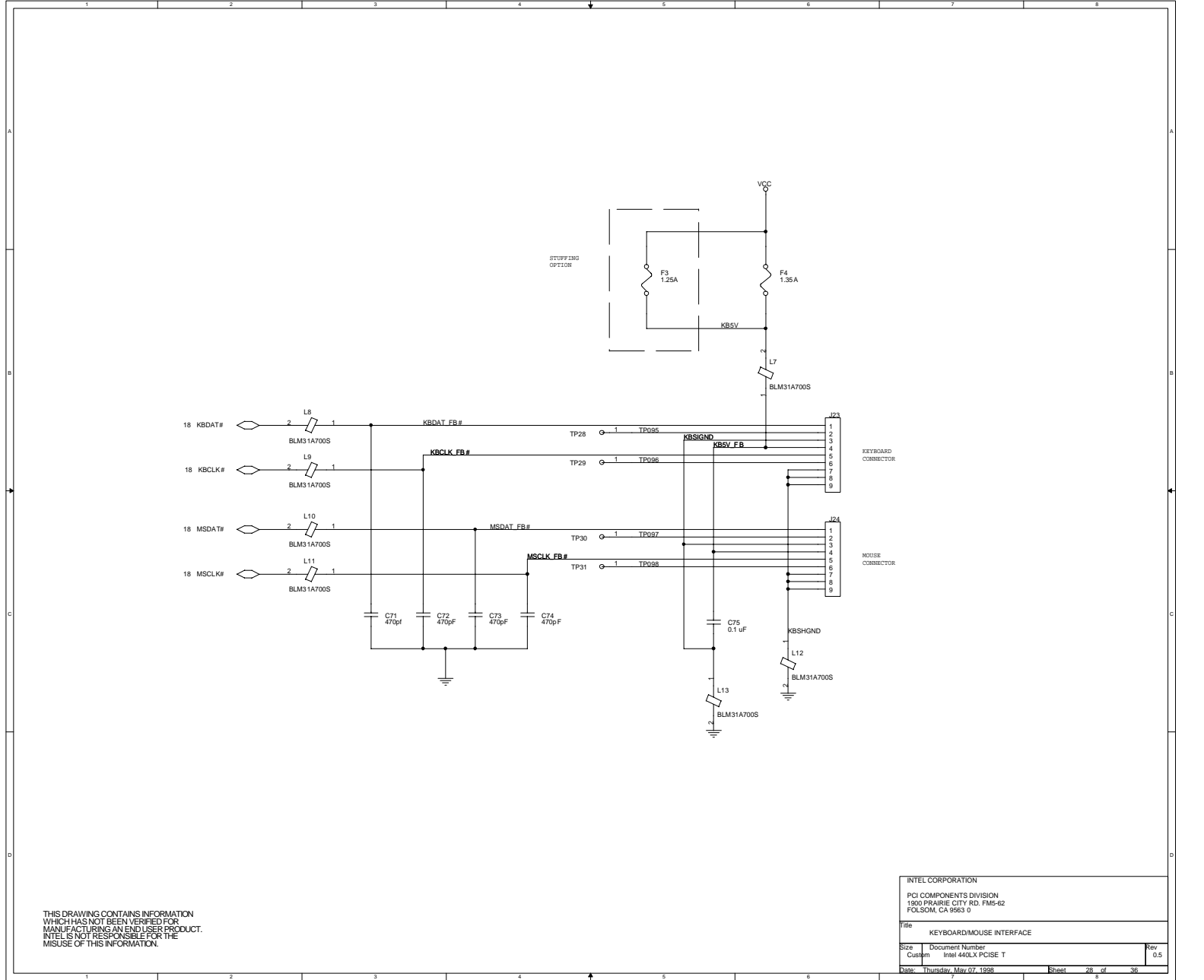


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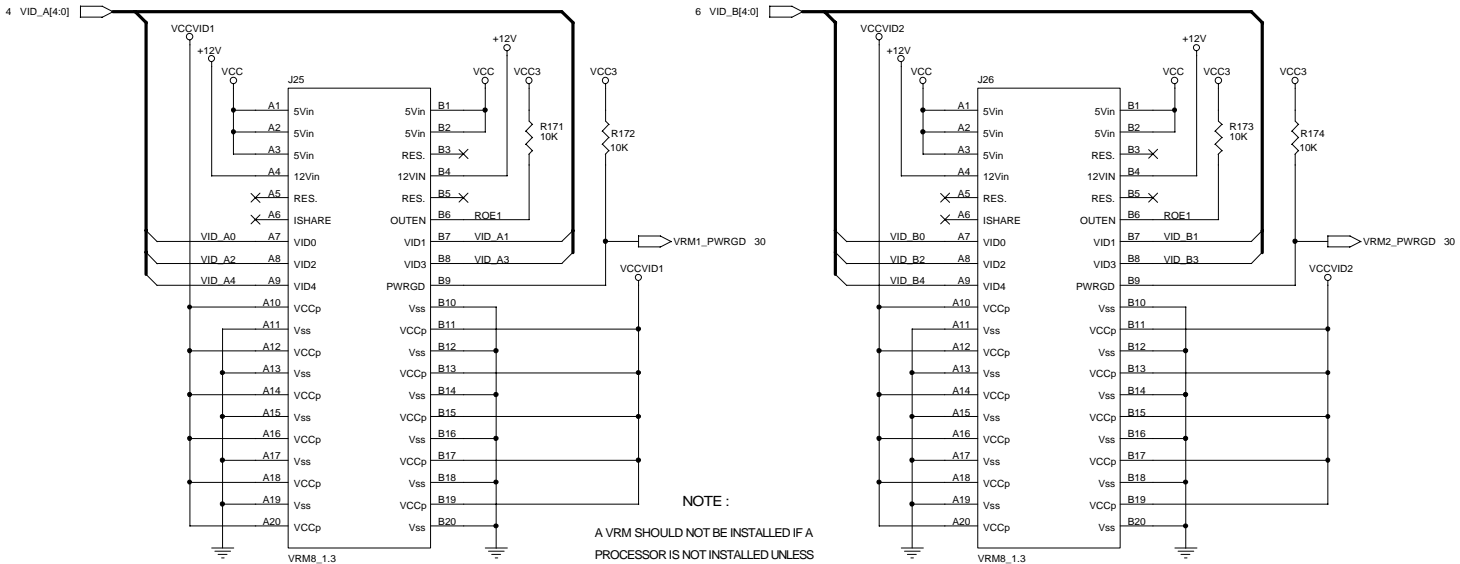
Title SERIAL AND FLOPPY

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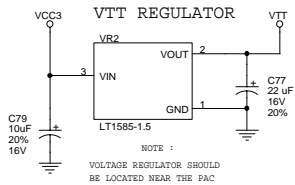


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Title	KEYBOARD/MOUSE INTERFACE	
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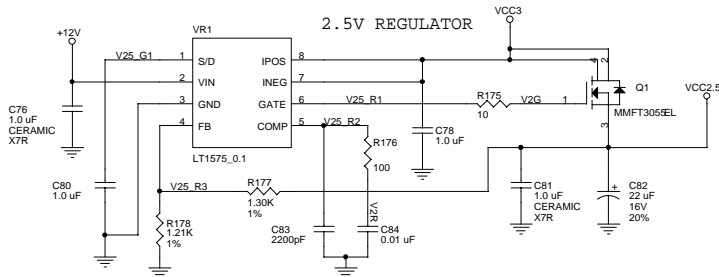


NOTE :

A VRM SHOULD NOT BE INSTALLED IF A PROCESSOR IS NOT INSTALLED UNLESS VRM_x_PWRGD IS ASSERTED BY THE VRM WITH A VID = 1111. IF NOT ASSERTED BY THE VRM, THEN CIRCUITRY MUST BE PROVIDED TO BLOCK VRM_x_PWRGD FOR THE UNPOPULATED SLOT 1.



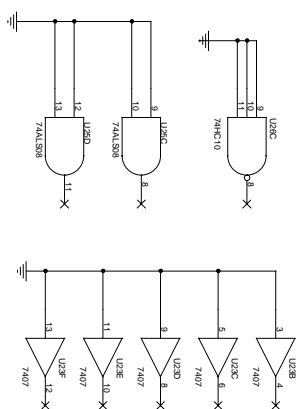
NOTE :
VOLTAGE REGULATOR SHOULD BE LOCATED NEAR THE PAC



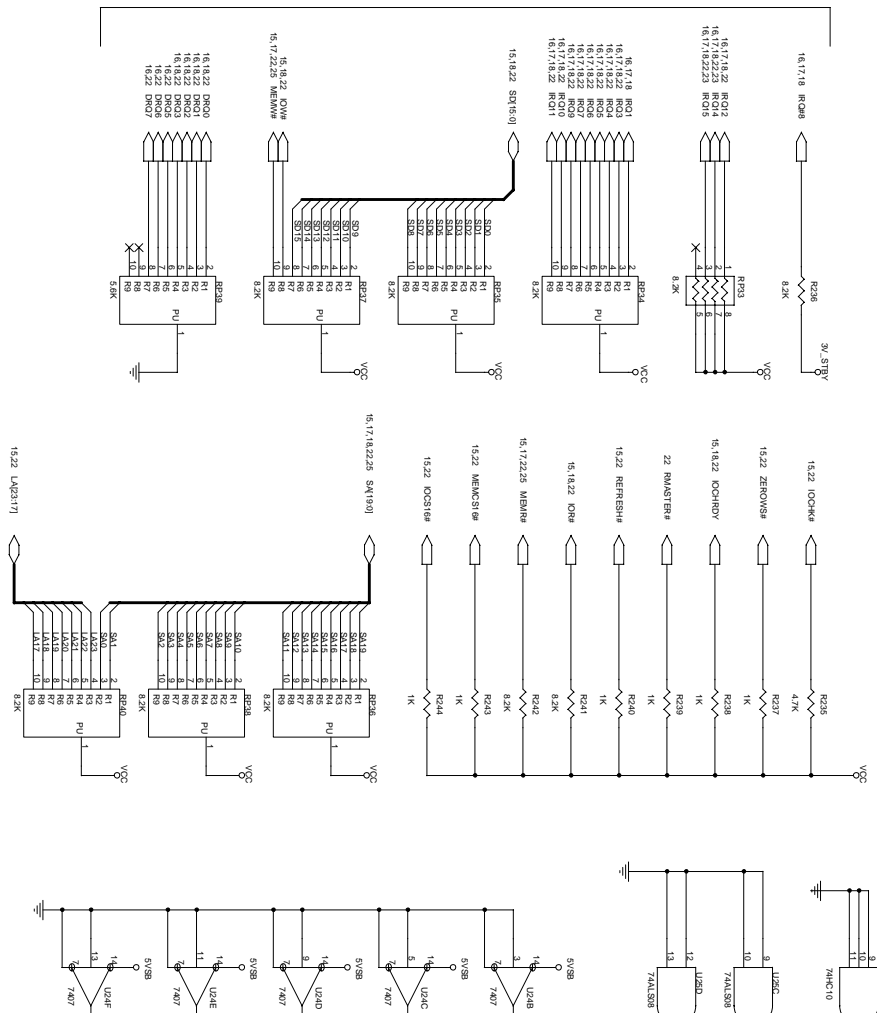
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Title DC-DC CONVERTER CONNECTORS		
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UNUSED GATES

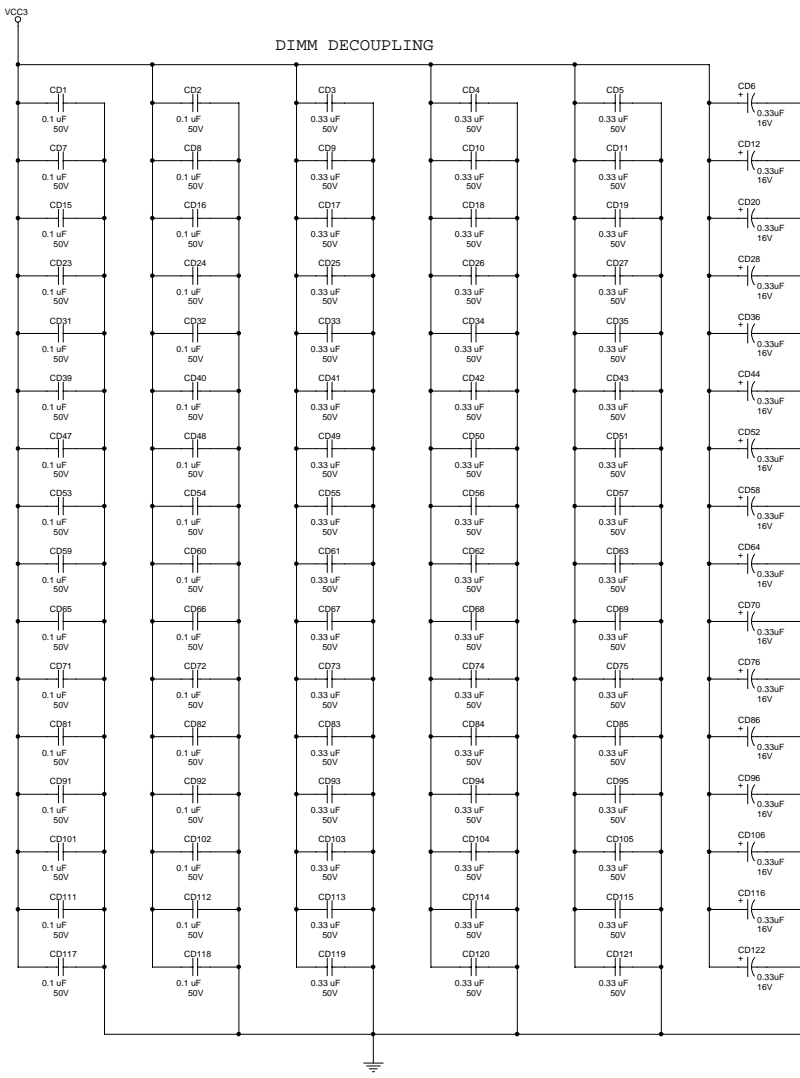


ISA BUS

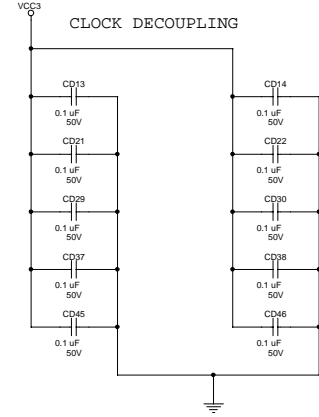


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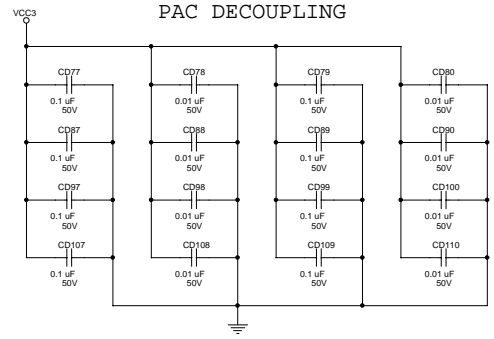
DIMM DECOUPLING



CLOCK DECOUPLING

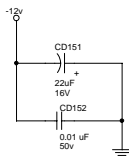
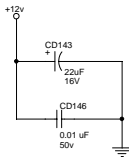
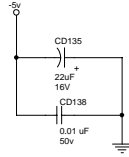
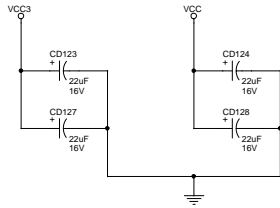


PAC DECOUPLING

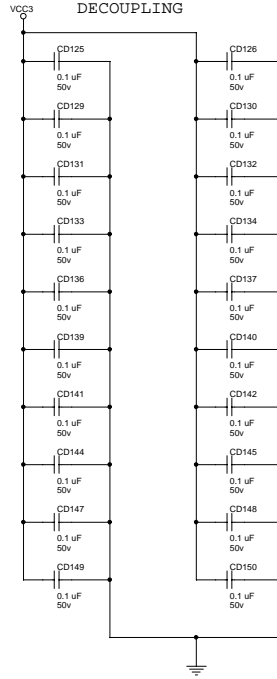


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BULK DECOUPLING



3 VOLT DECOUPLING

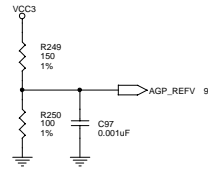
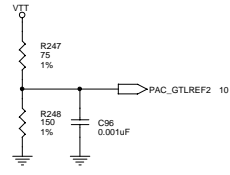
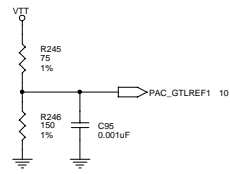
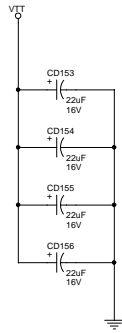


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File		
3.3 VOLT AND BULK POWER DECOUPLING		
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TERMINATION VOLTAGE DECOUPLING



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REVISION 0.5 - ADAPTED FROM REVISION 1.4 UP SCHEMATICS.

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Title Revision History		
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